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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,078	08/30/2001	Todd R. Abbott	MIO 0083 PA	7688

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EXAMINER

KIELIN, ERIK J

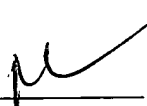
ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 11/15/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/943,078	Applicant(s) ABBOTT, TODD R. 	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 October 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) 17-38 and 40-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 10, 11 and 14-16 is/are rejected.
- 7) ☒ Claim(s) 8, 9, 12, 13 and 39 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
     If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
     a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4</u> | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of species I-A, claims 1-16 and 39 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that the restriction is improper for not indicating why the inventions are independent and distinct. This is not found persuasive because independentness and distinctness has been established by the various embodiments indicated in the instant specification and claims. Moreover, the restriction requirement filed 10 September 2002 states,

“Should applicant traverse on the ground that the species are not patentably distinct, **applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case.** In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.” (Emphasis added.)

If Applicant had believed that the inventions were not for some reason independent and distinct, then Applicant had the obligation to provide evidence or clearly state on the record that the inventions were not, in fact, independent and distinct. The absence of such a statement is taken to be an admission that Applicant believes the species to be independent and distinct. Accordingly, the argument is moot because Applicant appears to admit that the species are patentably distinct.

The traversal is also on the ground(s) that the restriction is improper because the species are not mutually exclusive. Examiner respectfully disagrees. A trench having the option of plural gates areas as well as the option of a plurality of local interconnect areas is a limitation which is mutually exclusive to a claim having the only a single gate area and a single interconnect area, because the limitations are different.

Applicant also appears to traverse the classification of invention II. While not commenting on the correctness of the classification, the invention may be classified in class 438, subclass 618, which is still different from 438/586. Accordingly, the different classifications for the inventions of I and II remain different and are still deemed to suggest different inventions with different searches.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 29-38, 40-41 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim, and claims 17-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim.

### ***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the gate area and the local interconnect area in the same trench (instant claims 1 and 39), the steps in the formation of the isolation region (instant claim 4), the silicide formed between the base substrate and the polysilicon within the local interconnect area of the trench (instant claim 12), and the steps of removing the polysilicon within the local interconnect area of the trench, forming the silicide therein and regaining-filling with polysilicon (instant claim 13), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

4. The disclosure is objected to because of the following informalities:

On p. 13, lines 1 and 2, it is indicated that cobalt is a silicide which is incorrect because cobalt is a metal. Appropriate correction is required.

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The process steps of claim 13 are not in the specification.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-16 and 39 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for forming a gate structure and an interconnect structure in *separate* trenches, does not reasonably provide enablement for forming a gate structure and an interconnect structure in the *same* trench. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

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Regarding independent claims 1 and 39, the drawings and the specification make it clear that the gate and the interconnect structures are formed in separate trenches 44 and 46, respectively. (See especially Fig. 10 and p. 11, second paragraph, which indicates that the gate and interconnect are formed in separate trenches 44 and 46, respectively and not in the same or a single trench.) The remaining claims are not enabled for depending from the independent claim 1.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim is considered indefinite because Applicant is using plural masks without identifying each separately. Language such as first mask and second mask should be used to make clear to which mask the step is referring.

### ***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b)

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only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

11. Claims 1-3, 5, 6, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,261,905 B1 (**Chen et al.**).

Regarding claims 1 and 10, **Chen** discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **440** (Fig. 3b) over a base substrate (col. 6, line 56 to col. 7, line 17);

forming a damascene trench **435** (Figs. 3b, 3c, 4a) in said first dielectric layer **440**, said trench having a gate area and a local interconnect area (col. 7, lines 18-21);

forming a gate oxide layer **430** (Fig. 3a) on said base substrate within said gate area of said damascene trench (col. 6, lines 44-46);

filling said damascene trench **435** with a conductive material **450, 470** which is polysilicon --as further limited by instant claim 10 (col. 7, 21-34 and col. 8, lines 12-18);

removing said first dielectric layer **440** to define a damascene gate structure **450, 470** and a damascene local interconnect structure **470** (col. 8, lines 16-22); note that the local interconnect structure is that formed over the isolation regions **410** as shown in Fig. 4d because it interconnects the control gates formed over each floating gate **450**.

Regarding claim 2, **Chen** forms isolation trenches **410** in the base substrate (Fig. 3a) before the formation of first dielectric layer **440**.

Regarding claim 3, a portion of the damascene trench **435** overlies the isolation trench **410** as shown in Figs 3c and 4a.

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Regarding claim 5, **Chen** shows the first dielectric layer 440 to be conformal (Figs. 3b and 4a).

Regarding claim 6, the damascene trench is formed by forming a patterned mask over the first dielectric layer 440, etching through the dielectric layer to the base substrate in areas defined by said patterned mask; and stripping said patterned mask (col. 6, line 62 to col. 7, line 9).

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** in view of **Wolf**, Silicon Processing for the VLSI Era, Vol. 2-Process Integration, Lattice Press: Sunset Beach CA, 1990, pp. 20-22, 39-41.

The prior art of **Chen**, as explained above, discloses each of the claimed features except for all of the details in the formation of the isolation trenches 410 but indicates that conventional methods should be used (col. 6, lines 30-35).

**Wolf** teaches a conventional method to form isolation trenches comprising,  
depositing a pad oxide layer over the base substrate (Fig. 2-26);  
depositing a nitride layer over the pad oxide layer;  
forming a mask over said nitride layer;

etching through portions of said nitride layer and said pad oxide layer and into said substrate defining an isolation trench opening in the substrate;

stripping away the mask; and filling the isolation trench opening with a dielectric material; and

removing the pad oxide and nitride.

(See pp. 39-41 for the general process --especially Fig. 2-26. Note that Wolf indicates that the pad oxide and nitride are etched as in the conventional LOCOS process which is discussed on pp. 20-22 especially at p. 21, section entitled "2.2.2.3 Mask and Etch Pad-Oxide/Nitride Layer to Define Active Regions.")

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the isolation trenches of **Chen** by the method in **Wolf** because **Chen** says that conventional methods should be used and because **Wolf** teaches notoriously well known conventional methods.

14. Claims 7, 11, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** in view of US 6,287,926 B1 (**Hu et al.**).

Regarding claim 7, the prior art of **Chen**, as explained above, discloses each of the claimed features except for forming an implant within said substrate through said damascene trench.

**Hu** teaches a method of forming a damascene gate wherein a channel implant **36** (Fig. 3) is performed in the damascene trench to form a channel stop region **34** (col. 6, last paragraph).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the channel stop in the invention of **Chen** in order to have a channel stop which are desired in the art, as taught by **Hu**.

Regarding claim 11, the prior art of **Chen**, as explained above, discloses each of the claimed features except for indicating if a silicide is formed over the polysilicon material within said gate area of said damascene trench.

**Hu** teaches forming a silicide 82 (Fig. 9) over the polysilicon of the gate region to reduce contact resistance (col. 10, lines 15-22).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the silicide over the gate region of **Chen**, to reduce contact resistance to the polysilicon gate, as is known in the art and as taught by **Hu**.

Regarding claim 14, the prior art of **Chen**, as explained above, discloses each of the claimed features except for forming lightly doped drain regions, after removing the first dielectric layer.

**Hu** discloses forming lightly doped source/drain (LDD) regions 86 after removing dielectric layer 16 (Fig. 9).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form LDD regions adjacent to the gates of **Chen** in order to complete the device of **Chen**, because a gate electrode must have a source/drain associated with it or it is not a transistor which would be contrary to the teachings in **Chen**.

Regarding claim 15, the prior art of **Chen**, as explained above, discloses each of the claimed features except for forming spacers against the vertical walls of the damascene gate structure and the damascene interconnect structure.

**Hu** forms spacers **64** against the gate structure **74** (Fig. 8).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form spacers against the gate of **Chen** in order to protect the sidewalls of the gate and further to provide spacing to form the heavily doped source/drain regions **76** as is known in the art to complete a transistor and as taught by **Hu**. One of ordinary skill would be motivated to form the spacers additionally to complete the device of **Chen**.

Regarding claim 16, the prior art of **Chen**, as explained above, discloses each of the claimed features except for forming the LDD regions after removing the first dielectric layer, forming spacers and forming the source/drain regions.

**Hu** as noted above teaches forming the LDD regions after removing the dielectric layer (Fig. 9) and forming the spacers adjacent the gate structure and forming doped source/drain regions in the substrate more deeply adjacent to the spacers than under the spacers. (It is noted that no order has presently been claimed that is not disclosed in **Hu**.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the LDD, spacers and source/drain regions in **Chen** in order to complete the transistors of **Chen**, because **Chen** teaches that it is known in the art to form source/drain regions (**Chen** prior art Fig. 1a) and because the method of **Hu** is conventional for forming LDD regions and source/drain regions using the spacer for spacing the source/drain regions relative to the LDD regions.

*Allowable Subject Matter*

15. Claims 8, 9, 12, 13, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter:

Claims 8, 9, and 39 are considered allowable because the prior art of record does not teach or suggest, in combination with the other claimed features, the forming of a contact opening to a base substrate by growing and then etching through an oxide layer formed in the trench, in the local interconnect area, of a **single** trench having **both** a gate area and a local interconnect area.

Claims 12 and 13 are considered allowable because the prior art of record does not teach or suggest, in combination with the other claimed features, forming a silicide between the base substrate and the polysilicon of the local interconnect region of a **single** trench having **both** a gate area and a local interconnect area.

*Conclusion*

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 3,891,190 (**Vadasz**), US 6,083,827 (**Lin** et al.), and US 5,599,728 (**Hu** et al.) each disclose, at least, each of the features of the instant claim 1 except for removing the first dielectric layer. Note that although Hu does not show the local interconnect in the figures, Hu.

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states that the interconnect is formed simultaneously with the gate structure (Hu col. 4, lines 29-34).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Erik Kielin  
November 14, 2002